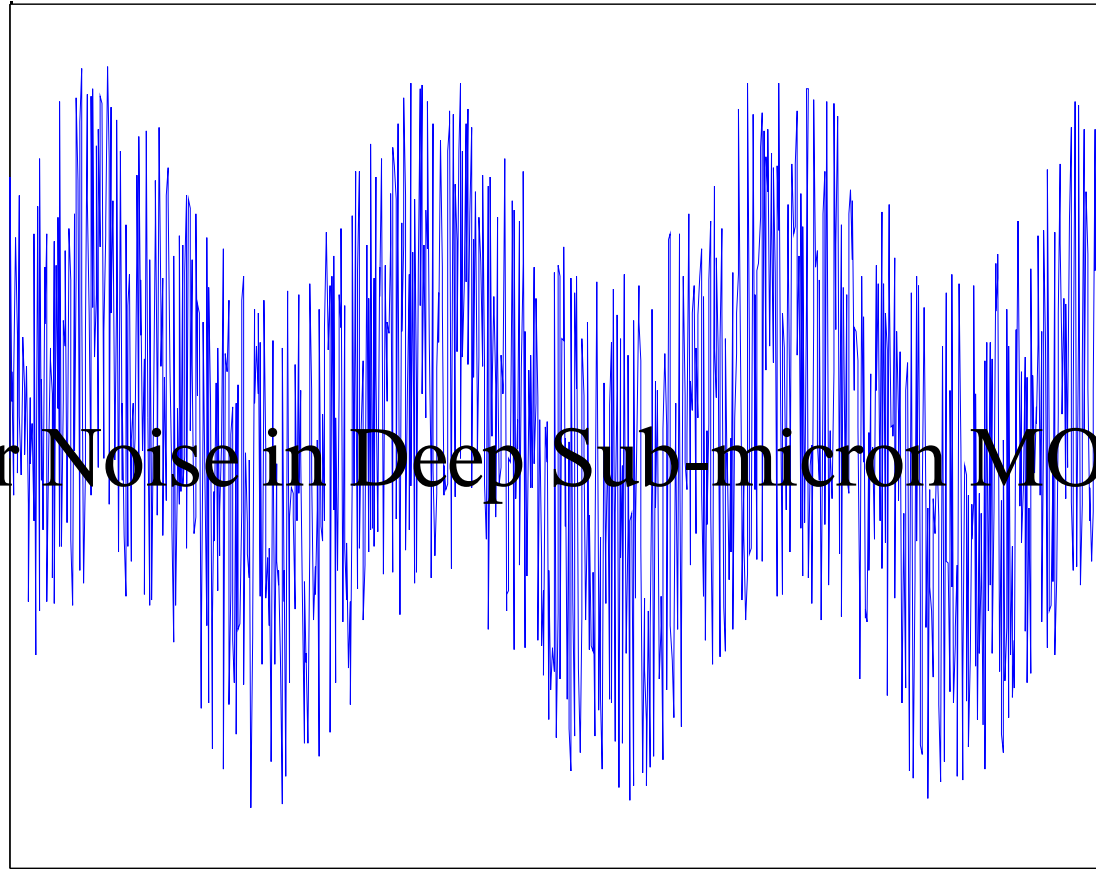


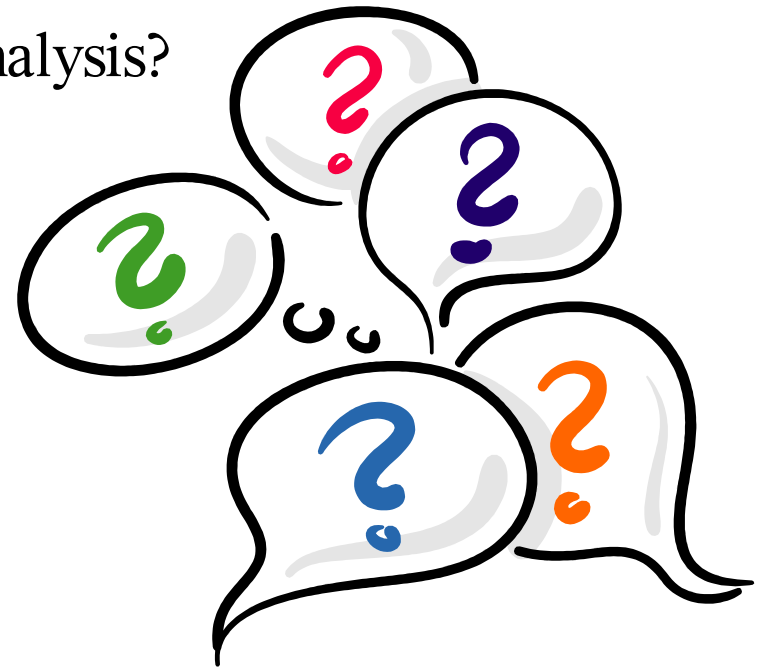
NOISE MODELING & SIMULATION

Flicker Noise in Deep Sub-micron MOSFETs



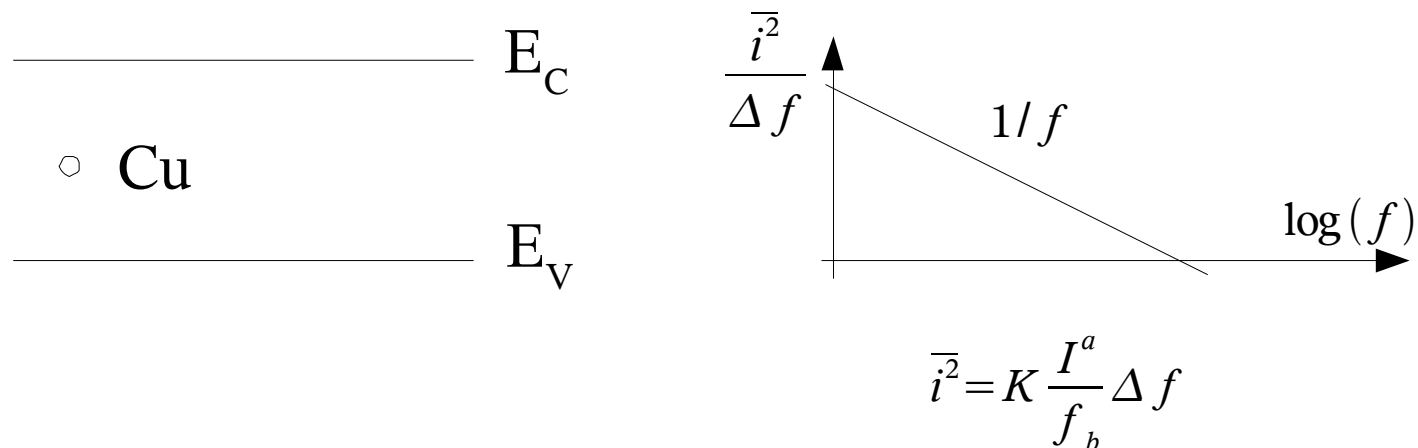
CIRCUIT DESIGNERS: WHAT DO WE NEED TO KNOW?

- Three key questions:
 - What exactly IS (flicker) noise?
 - How does it affect circuit operation (noise analysis)?
 - What are the pitfalls with noise analysis?



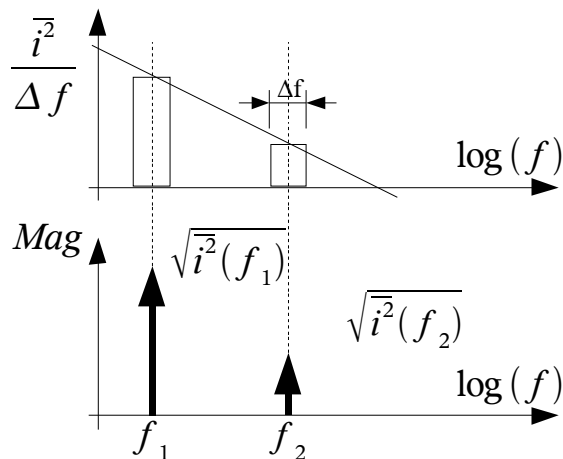
WHAT IS FLICKER NOISE?

- Caused by traps in semiconductor material
 - Due to contamination or crystal defects
- Has a $1/f$ power spectral density

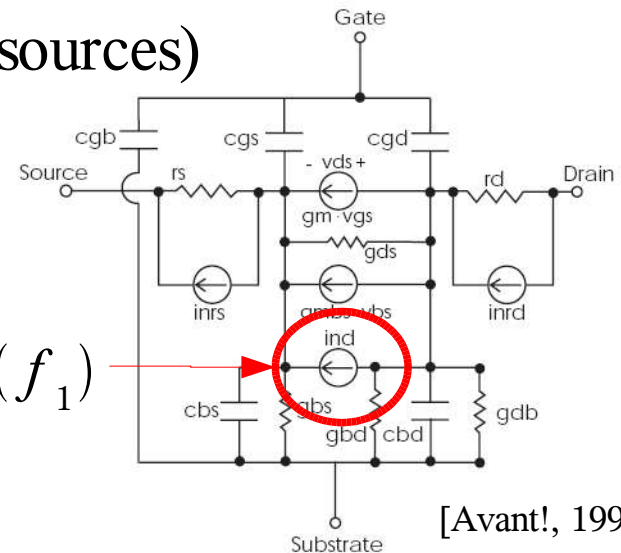


NOISE ANALYSIS

- Done with conventional (AC) circuit analysis techniques
 - Superposition principle
 - POWER is summed (non-correlated sources)

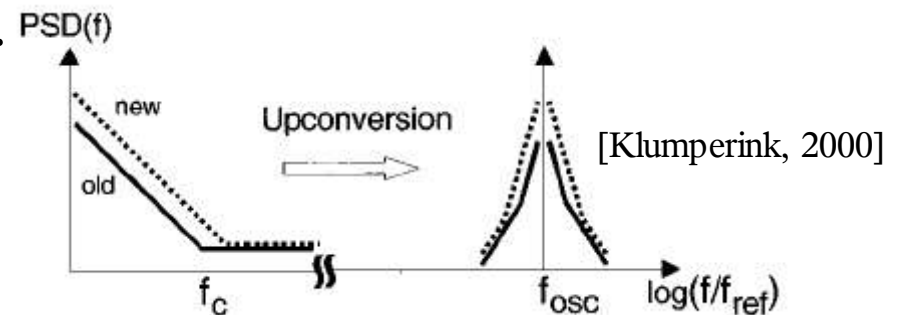


$$\sqrt{i_{fl}^2 + i_{th}^2}(f_1)$$



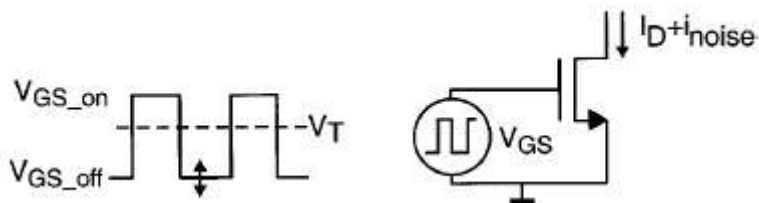
[Avant!, 1999]

- Easily predict noise behaviour
 - Ex: upconversion

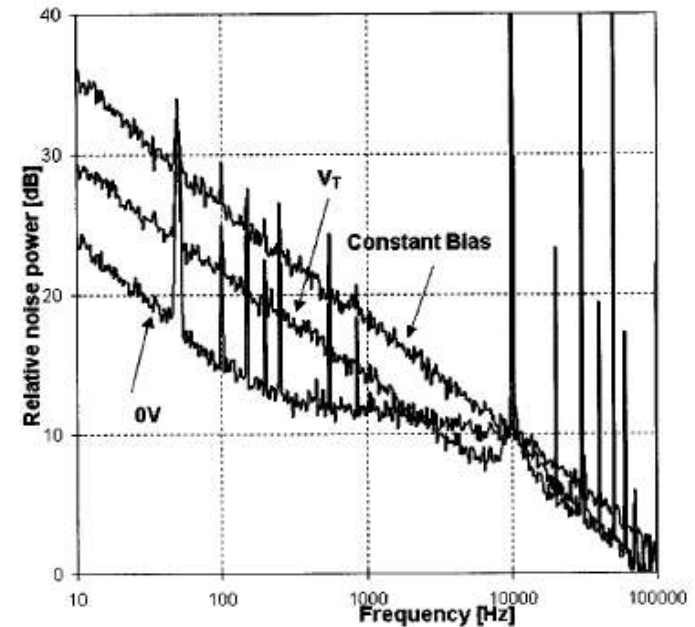


REDUCING 1/f NOISE

- Can we reduce 1/f noise?
 - Switched biasing reduces 1/f noise - reason is unknown
- New questions:
 - How do we simulate this effect?
 - How do we invent new techniques?
- For answers:
 - What IS noise?



[Klumperink, 2000]



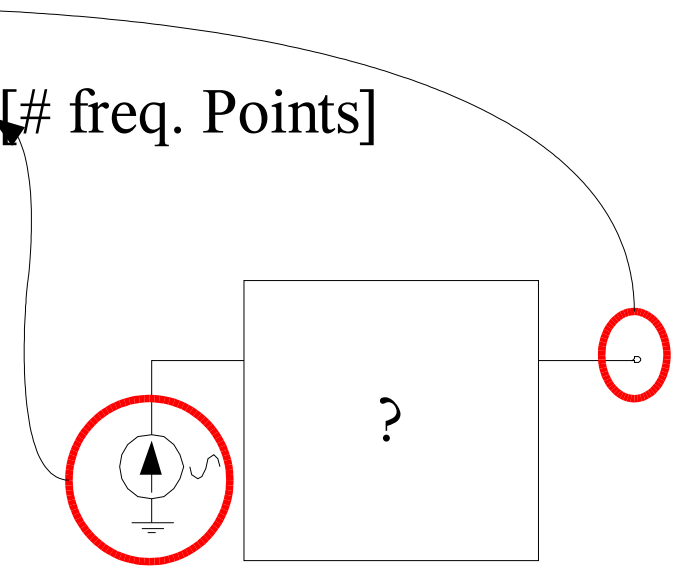
NOISE SIMULATIONS

- HSPICE Analyses:

- .NOISE [output node] [input I/V source] [# freq. Points]
- .SAMPLE: for noise folding analysis

- HSPICE Outputs:

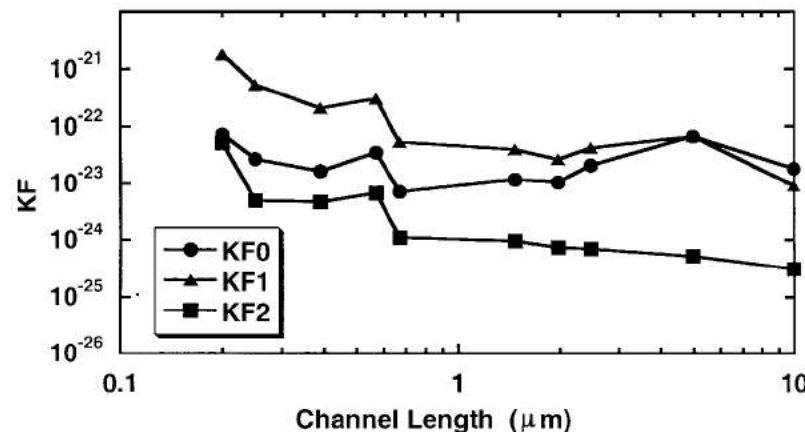
- .PRINT NOISE [INOISE] [ONoise]
- .PLOT NOISE [INOISE] [ONoise] [...]
- .GRAPH: high resolution plots
- .PROBE NOISE [INOISE] [ONoise]



BASIC SPICE FLICKER MODELS FOR MOSFET CHANNELS

- Want to ensure accurate L dependance of models
 - Benchmark: KF parameter

NLEV	0	1	2 & 3
PSD	$\frac{\overline{i_{fl}^2}}{\Delta f} = \frac{KF0 \cdot I_D^{AF}}{C_{OX} L^2 f}$	$\frac{\overline{i_{fl}^2}}{\Delta f} = \frac{KF1 \cdot I_D^{AF}}{C_{OX} L W f}$	$\frac{\overline{i_{fl}^2}}{\Delta f} = \frac{KF2 \cdot g_m^2}{C_{OX} L W f^{AF}}$



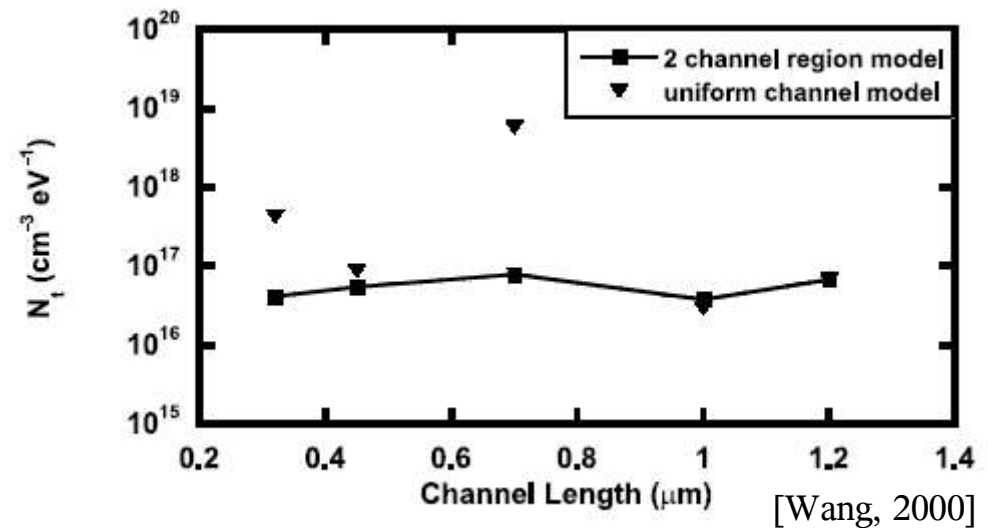
[Çelik-Butler, 1999]

- All bad models for deep sub-micron (No $1/L^3$ dependance)



BSIM FLICKER MODEL FOR MOSFET CHANNELS

- Again, want to ensure accurate L dependance of models
 - New benchmark for BSIM3: trap density (N_t)
- Problem
 - Non-constant N_t
- Solution*
 - Dual V_T model (for MDD & channel regions)



*Solution is not yet implemented (BSIM4 uses same model as BSIM3)



CONCLUSION: SHOULD WE EVEN TRY?

- Even with these problems, we can still use noise simulations as a guide. Simply be conscious:
 - For what devices are the models valid?
 - Noise simulations for small devices underestimate noise
 - Use larger devices with known characteristics if possible
- More effort should be put in understanding noise
 - Simulation results will be more accepted by designers
 - Might even find simple ways to reduce noise



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